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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/815,137	03/31/2004	Murray Steven Rodgers	50060-00145	9201

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EXAMINER	
AU, BAC H	

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 03/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/815,137	RODGERS ET AL.	
	Examiner	Art Unit	
	Bac H. Au	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *31 March 2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-2, and 4-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Cronin (U.S. Pat. 4776087).

Regarding claim 1, Cronin [Figs.6-11] discloses a method for making a shielded multi-conductor interconnect bus comprising the steps of:

removing portions of a first layer of dielectric material [50,54] overlying and supported by at least a portion of a substrate to provide a plurality of parallel channels in the first layer of dielectric material;

depositing a first layer of electrically conductive material [56] over the first layer of dielectric material, the first layer of electrically conductive material filling the channels formed in the first layer of dielectric material;

removing strips of the first layer of electrically conductive material to provide a plurality of electrically conductive lines [56A] on the first layer of dielectric material extending parallel with the channels formed in the first layer of dielectric material, wherein an upper surface of the first layer of dielectric material is exposed at the bottom of each strip;

depositing a second layer of dielectric material [58] over the first layer of electrically conductive material, wherein the second layer of dielectric material fills the strips removed from the first layer of electrically conductive material;

removing portions of the second layer of dielectric material to provide a plurality of parallel channels in the second layer of dielectric material, the channels in the second layer of dielectric material being located to overlie the filled channels in the first layer of dielectric material and extending downward through the second layer of dielectric material to expose the first layer of electrically conductive material filling the channels in the first layer of dielectric material [Fig.9]; and

depositing a second layer of electrically conductive material [60] over the second layer of dielectric material, wherein the second layer of electrically conductive material fills the channels formed in the second layer of dielectric material.

Regarding claims 2 and 4-7, Cronin discloses a method

wherein in said step of removing portions of a first layer of dielectric material, the substrate is comprised of silicon [Col.4 lines 13-19] and the first dielectric layer comprises a dielectric stack layer [50,54] covering an upper surface of the substrate comprising a lower layer of thermal oxide [Col.4 lines 7-10] and an upper layer of silicon nitride [Col.4 lines 33-36];

wherein in said steps of removing portions of a first layer of dielectric material and removing strips of the first layer of electrically conductive material, the portions are

removed in a manner providing channels and strips arranged in a pattern wherein one of the channels is located between sets of the electrically conductive lines, each set of electrically conductive lines including at least one electrically conductive line [Fig.8];

wherein in said step of depositing a second layer of dielectric material, the dielectric material comprises one of silicon dioxide and silicate glass [Col.4 lines 7-10; col.5 lines 1-2];

wherein in said step of depositing a first layer of electrically conductive material [56], the electrically conductive material comprises doped polysilicon [Col.4 lines 10-13, 56-62];

wherein in said step of depositing a second layer of electrically conductive material [60], the electrically conductive material comprises doped polysilicon [Col.5 lines 15-19].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cronin (U.S. Pat. 4776087) in view of Sun (U.S. Pat. 5262353).

Regarding claim 3, Cronin implies in the method wherein in said step of removing portions of a first layer of dielectric material, sufficient material is removed to provide channels in the first layer of dielectric material that extend vertically downward through the first layer of dielectric material to expose the upper surface of the substrate along at least a portion of each channel, where electrical contact is required between metallization layers and active regions of the substrate. Cronin does not show or expressly disclose this limitation; however, Sun [Fig.1] discloses in the method wherein in said step of removing portions of a first layer of dielectric material [14], sufficient material is removed to provide channels in the first layer of dielectric material that extend vertically downward through the first layer of dielectric material to expose the upper surface of the substrate [12] along at least a portion of each channel.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Sun into the method of Cronin to include in the method wherein in said step of removing portions of a first layer of dielectric material, sufficient material is removed to provide channels in the first layer of dielectric material that extend vertically downward through the first layer of dielectric material to expose the upper surface of the substrate along at least a portion of each channel. The ordinary artisan would have been motivated to modify Cronin in the manner set forth above for at least the purpose of providing electrical contact from the metallization layers to active regions of the substrate.

3. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cronin (U.S. Pat. 4776087) in view of Fitch (U.S. Pat. 5324683).

Regarding claim 8, Cronin [Fig.10] discloses in the method wherein said step of depositing a second layer of electrically conductive material comprises the steps of:

depositing a lower layer of doped polysilicon [57]; and

depositing an upper layer of doped polysilicon [60].

Cronin fails to disclose wherein said step of depositing a second layer of electrically conductive material comprises the steps of: depositing an intervening layer of sacrificial material; and removing the intervening layer of sacrificial material.

However, Fitch [Figs.12-15] discloses in the method wherein said step of depositing a second layer of electrically conductive material comprises the steps of: depositing an intervening layer of sacrificial material; and removing the intervening layer of sacrificial material [Col.8 lines 16-21].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Fitch into the method of Cronin to include in the method wherein said step of depositing a second layer of electrically conductive material comprises the steps of: depositing an intervening layer of sacrificial material; and removing the intervening layer of sacrificial material. The ordinary artisan would have been motivated to modify Cronin in the manner set forth above for at least the purpose of forming an air gap region to provide optimal low-K dielectric region [Fitch; col.7 line 67 – col.8 line 1].

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Bac H. Au whose telephone number is 571-272-8795. The examiner can normally be reached on Mon-Fri 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on 571-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BHA

Zandra V. Smith
Supervisory Patent Examiner
March 10, 2006